Review: Recent Directions in ECG-FPGA Researches

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Abstract

The last few years witnessed an increased interest in utilizing field programmable gate array (FPGA) for a variety of applications. This utilizing derived mostly by the advances in the FPGA flexible resource configuration, increased speed, relatively low cost and low energy consumption. The introduction of FPGA in medicine and health care field aim generally to replace costly and usually bigger medical monitoring and diagnostic equipment with much smaller and possibly portable systems based on FPGA that make use of the design flexibility of FPGA. Many recent researches focus on FPGA systems to deal with the well-known yet very important electrocardiogram (ECG) signal aspects to provide acceleration and improvement in the performance as well as finding and proposing new ideas for such implementations. The recent directions in ECG-FPGA are introduced in this paper.

Keywords: FPGA, ECG, Security, Compression, Denoising, Detection, Diagnose, Medicine and Health Care.

1- Introduction

The electrocardiogram (ECG) signal is a recording related to the heart electrical activity. The ECG signal provides critical information for heart health state and even heart diseases. The ECG signal preprocessing and analyzing take a large deal of the past and recent health and medical researches due to its important role and influence over the diagnose decision which can make the difference of saving patient life in many situations, The ECG signal give an information about heartbeat rate, heart abnormalities as well as biometric identification [1-3].

The last few years have shown an evolution in the utilization of FPGA for a variety of applications in many fields. For example, FPGA was implemented to deal with pedestrian detection for the monocular detection system [4], transient disturbance detection in the power system [5], dual three-phase induction machine (DTPIM) simulator implementation in machine systems [6] and many other fields. Meanwhile, the researchers in health care and medical field give great attention to FPGA due to its promising performance, affordable price alongside with its design flexibility, relatively low power consumption and lightweight. Due to these reasons, the FPGA based implementations in health care and medical field was widely adopted mainly to provide a high-speed hardware approach. Nevertheless, another direction was focused on utilizing FPGA to introduce a suitable wearable device capable of wirelessly transmitting updated information of patient health. The recent research directions in ECG-FPGA systems focus on many important aspects of ECG signals, which include security, compression, denoising, detection and diagnose as illustrated in Figure (1).

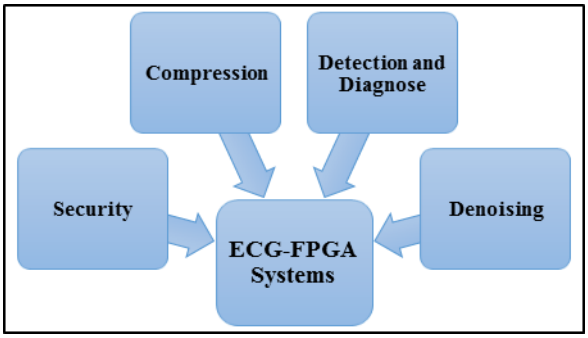

Figure (1) the recent research directions in ECG-FPGA systems.

The rest of the paper is organized as follows: Section 1 includes the recent methods applied in the ECG-FPGA security field. The ECG-FPGA compression implementation methods are included in Section 2. In Sections 3, the denoising implementation of ECG-FPGA is reviewed. Section 4 focused on the detection and diagnostic implementation of the ECG-FPGA. Lastly, the conclusions of the paper are presented.

2- Recent ECG-FPGA Research Directions

1) Security Implementation

In recent years, a part of the ECG researches interest was focused on the security issues related to the secure transmission of ECG information, the protecting of personal patients' ECG information, and in general preventing the unauthorized access to ECG signals records. In turn, some of these researches introduce and suggest FPGA based systems to provide efficient solutions that can deal with these security issues in hardware efficient manner.

The researchers in [7] suggest a simple partial selective encryption scheme for the ECG signal security purposes. The proposed encryption scheme applied on half of the total number of ECG sampled data and utilize algebraic addition and subtraction to perform frequency band separation in manner similar to filter bank technique of DWT. The other half of ECG sampled data remain unencrypted and used alongside the encryption part to construct the final encrypted ECG signal. The proposed scheme was implemented on Xilinx Virtex4 and Xilinx Spartan 3 XC3S50 FPGA platforms. The results suggest that a

noise like behavior is obtained for the final encrypted ECG signal with correlation coefficient very close to zero. The research suggests that the proposed scheme simplicity lower the required computation effort cost of the FPGA implementation as well as boosting the processing speed of encryption.

The researchers in [8] presents FPGA-based implementation based on the Advanced Encryption Standard (AES) algorithm and ECG identification system that aims to transmit and save ECG signals securely in real-time manner. The proposed system was implemented on the Xilinx ZC702 evaluation board. The obtained results suggest the proposed implementation provide a fast response with low resource usage and power consumption.

In [9], the research deal with the encryption and decryption of patient ECG signals records to provide a fast and secure transmission of ECG signals that block the access of non-allowed persons. The research suggests an improved architecture of AES Algorithm that reduces the time required to generate sub-keys of the key expansion process. The improved architecture of AES is simulated and then realized on a Virtex 5 XC5VLX50T FPGA platform to get better security with respect to that of based on software. The results obtained by [9] suggest the improved architecture applied to FPGA was faster and reduce the time to about half comparing to that of original AES while the resource area and consumed power are almost the same.

2) Compression Implementation

The compression and transmission challenges related to a large amount of ECG signals data, which required relatively large processing resources and time, draw increasing attention. Approaches based on FPGA were proposed to obtain sufficient hardware implementations that provide a fast ECG data compression.

The researchers in [10] suggest an improvement to existing fast linear approximation distance threshold (LADT) that reduce computation complexity of ECG signal compression in real-time manner. The suggested improved fast LADT was simulated in Matlab and then realized on FPGA XC3s400 platform. The results shown in [10] suggest a good performance of the FPGA implementation.

In [11], the research presents a simple structure compression approach for ECG signal. The compression utilize delta coding with a separation and rotation mechanism to provide a reduction in values variation of the ECG signal. The delta coding is followed by run length encoding (RLE) for zero bit that eliminates the zero level sections in the ECG signal. The researchers claim that the proposed approach implementation on FPGA give a correct compression performance while the FPGA resource usage kept low.

3) Denoising Implementation

The ECG signals usually suffer from different types of noise and interference that make it difficult to extract reliable information of them. This in turn motivated several researchers to introduce variety of approaches to remove, or at least reduce, the noise effect effectively alongside hardware implementation based on FPGA that provide flexibility in design and performance.

In [12], a FPGA implementation was proposed to filtering the ECG signal using dual FIR filter to improve the ECG filtering performance. The proposed implementation was realized on a ALTERA's cyclone EP1C12Q240C8 FPGA platform.

The researchers in [13] utilize wavelet transformation along with Fast Fourier Transform (FFT) to perform filtering operation over the ECG signal. The work was realized on Altera Cyclone III 3C16 FPGA platform. The obtained results suggest that Fast Fourier Transform and Wavelet Threshold De-noising can reduce the noise as desired.

The researchers in [14] used FIR filter based on distributed algorithm approach to perform filtering over the ECG signal. The distributed FIR filter implemented based on Alter Cyclone III FPGA platform and simulated by the Quartus II and Matlab. The research results suggest that the approach provide good filtering to the ECG signal.

The researchers in [15] introduce a real-time FPGA-based implementation with parallel architecture that utilizes the Least Mean Square (LMS) algorithm to remove power-line interference from ECG signal. The implementation was realized over on Xilinx XUPV5 Development Board.

With the aim of eliminating the power line interferences from the ECG signal, the research in [16] present a FPGA realization for an adaptive filter based on the LMS algorithm. The filter was realized on DE2 board that contains a Cyclone II FPGA chip. The results obtained of the proposed FPGA realization suggest that it is suitable for real-time robust ECG filtering.

In [17], a hardware approach based on FPGA was introduced that firstly perform denoising to ECG signal using FIR filter, then detect of heartbeat using a modified Pan and Tompkins algorithm proposed in [18]. The approach was carried on ALTERA DE II FPGA platform. The research results suggest that the approach detection performance has high level of accuracy in real-time manner.

In [19], show a cascade implementation of FIR filter that utilizes hamming and rectangular windowing methods to perform ECG signal denoising. The cascade implementation was carried on Vertex-6 FPGA platform. The researchers suggest that the FPGA realization performance is better in removing the baseline wanders (BLW) and the power line noise within an acceptable power and resource usage range.

The researchers in [20] show an FPGA realization that utilizes a single multiband FIR least squares type filter to eliminate interference signals related to power system, respiration, muscle and white noise at different frequencies. The FIR filter realized on Terasic DE2-70 board that contains Alter Cyclone II EP2C70F896C6 FPGA chip.

In [21], a pipelined-based delayed error normalized LMS adaptive filtering approach is applied to denoise the ECG signal. The presented approach was realized over Virtex5 XC5LVX330 FPGA platform. The results presented in this research suggest that the FPGA realization of the proposed approach give a fast enhanced denoising performance with lower power consumption but in an expanse of the need for greater area resources and slightly increase in computational complexity comparing to conventional algorithms.

4) Detection and Diagnostic Implementation

A great deal of ECG research efforts was directed to enhance the detection and diagnostic of ECG monitoring systems. Many researchers suggest FPGA based systems that can achieve high detection sensitivity and fast response alongside with ability to provide portability, real-time performance as well as low affordable cost.

The researchers in [22] presents FPGA implementation to monitor ECG signal in real-time manner that include the functionality of filtering and QRS detection. The proposed system was implemented on a Spartan-3 XC3S400-4TQ144C FPGA platform. The results obtained by [22] suggest the proposed FPGA implementation provide a stable real-time ECG signal monitoring performance.

In [23], the researchers propose a FPGA implementation for QRS complexes detection based on wavelet signal processing method called an Adaptive Lifting Scheme (ALS). The FPGA used in this work was Xilinx's Virtex II Pro XC2VP30 FPGA platform. The obtained results of FPGA implementation was compared to that obtained by implement ALS method over TI's DSP TMS320VC5509A system in C language. Based on the results, the research gives a conclusion that the QRS detection performance using ALS-FPGA approach introduce an effective time reduction compared to the ALS-DSP system approach while maintaining the highly accurate detection rate.

In [24], show a hardware/software implementation based on FPGA that perform QRS detection and beat classification of ECG signal. The proposed implementation was carried out over Virtex II PRO XC2VP30-FF896-7 FPGA platform. The hardware QRS detection part is based on an algorithm that utilizes a phase-space portrait of ECG signal, while another algorithm from the Open Source ECG Analysis Software (OSEA) is used to carry out the beat classification part. The reported results show a high sensitivity and positive productivity performance in QRS detection and premature ventricular beat detection and also claim that the hardware/software implementation processes the ECG data in a much higher processing speed compared to that depending only on software implementation.

In [25], the researchers present an online R and T peak detection method based on their previous work proposed in [26] that deal with the QRS detection from ECG signal. The R and T detection method based on slope detection was realized on Xilinx Spartan3 xc3s400tq144-5. The results of the work indicate that performance obtained by the FPGA realization was fast with highly promising detection sensitivity for both R and T peak detection.

The researchers in [27] present an online portable monitoring system aim to analyses the heart rate variability (HRV) of ECG complex signal. The architecture of the proposed system divided into two sides (patient side and pc mobile side) that connected wirelessly via Bluetooth. The proposed ECG monitoring system was realized with Cheetah ARM SoC platform solution as System on Chip - Field Programmable Gate Array (SoC-FPGA) embedded computing platform. The research results conclude that the system realization provides highly integrated performance with wireless capability at low cost.

The researchers in [28] show a real-time FPGA implementation for QRS detection that utilizes a pipeline architecture and based on ALS. The system was realized on Virtex 5 XUPV5-LX110T evaluation FPGA platform. The work results indicate that FPGA implementation performance has high detection accuracy while maintain low power consumption.

In [29], present a FPGA approach to deal with ECG signal processing and R peak detection of cloud clients connected to tele-health server. The research results suggest that proposed approach offer efficient FPGA resource reduction and fast response suitable for real-time implementation.

In [30], propose FPGA realization that utilizes the Discrete Wavelet Transform (DWT) based on Mallat algorithm to minimize the required resource usage and speed out the computations. The proposed approach was applied to detect QRS complex and remove the BLW. Due to resources limitations, the entire system was simulated on Xilinx ARTIX 7 XC7Al00T and the BLW suppression part was tested using JTAG Hardware co-simulation on Spartan-6 XC6SLX16 FPGA platform. The results of [30] were visually evaluated and the research suggests that the BLW part was carried successfully while claiming that despite of the good performance of QRS detection part it wasn't able overcome yet the batter performance of linear filtering implementation obtained by their past work in [31].

With the aid of the previous work in [31], the research in [32] presents an FPGA-based Multiprocessor System on Chip (MPSoC) implementation in master-slave fashion to detect QRS complex of the ECG signal. The research utilizes and tests a reduced 3-processor configuration that consists of a master processor that provide the system control and two slave processors that handle the 12-lead ECG standard. The proposed configuration was carried out over Xilinx Spartan6 XC6SLX16 FPGA platform.

In [33], present FPGA realization aims to detect QRS complex and utilized it for ventricular and supraventricular tachycardia diagnosis in real-time manner. The research applies the fuzzy entropy measure of high resolution ECG sample values to neural network. The suggested diagnostic system based on fuzzy neural is realized on Altera EP1C6Q240C8 FPGA platform to take advantage of FPGA low cost and flexibility to map changes in the proposed algorithm. According to the results obtained by [33], the applied fuzzy neural FPGA based realization was fast with very high detection accuracy comparing to other QRS methods detection.

The work presented in [34] focuses on providing a hardware FPGA-based realization that performs preprocessing to the ECG complex signal as well as detecting R wave and heart beat value. The proposed FPGA realization firstly performs denoising ECG signal using bandpass FIR filter followed by corrosion and inflation operations as morphology transform of the ECG signal and then R wave detection stage with an updated threshold set is carried out. The FPGA implementation is realized on Xilinx Spartan-6 XC6SLX45T FPGA platform. The obtained results suggest that the performance and the detection of R wave was fast, accurate and consume small amount of power.

The researchers in [35] suggest an alternative approach to that of [32] which consist of a three stages algorithm inspired by [36] to detect the QRS of the ECG complex signal. The first stage of proposed algorithm performs filtering operation using high-pass and low-pass FIR filters to eliminate noise, interference as well as P and T waves from the ECG signal. To reduce the rate of misleading detection, the second stage performs differentiation, non-linear transformation and integration. The final stage uses a

fixed window size to maximums search with amplitude and time thresholds to perform the QRS detection. The algorithm is tested using Matlab and realized on Altera DE2-115 board that contains a cyclone IV 4CE115 FPGA chip. The results in [35] claim a high rate of successful detection that overcome the FPGA-based performance of [32] without excluding the challenging ECG signals of the same tested database.

The researchers in [37] propose an adaptive window size detection approach to enhance the work in [35].

In [38], a Bluetooth wireless heart rate and body temperature monitoring FPGA-based system were introduced. The Pan Tompkins algorithm is used for QRS complex detection and the resulted heart rate calculations. The proposed system realizes over SoC FPGA-based Zynq development board. The results suggest that the system is reliable with successful extract performance.

In [39], a remote ECG monitoring system was proposed that utilize the Two-level Load-balance Monitoring Strategy (TLLBMS) to lower delay time and increase reliability performance. To carry this task, the ECG monitoring system realizes parallel Principal Component Analysis - Independent Component Analysis (PCA-ICA) algorithm and Message Digest Hash Algorithm MD5 over the System-on-Chip A2F500 FPGA-based board. The research results suggest that the system has high level of practicality in providing reliable performance with very small delay time.

FPGA realization was presented in [40] that based on a low complexity detection and identification approach of P, R and T peaks from a noise free ECG signal using histogram algorithm. The FPGA implementation is carried on Virtex-5 XC5VLX50TFF G1136C FPGA platform. The researchers suggest that the implementation make use of the proposed approach simplicity to give a fast performance with better and accurate values comparing to the other approaches.

In [41], the researchers present a study on FPGA implementation based on artificial neural network (ANN) to perform an ECG anomaly detection. The resilient backpropagation (RPROP) is used as neural network training algorithm for its generalization ability. The Principal Component Analysis method is carried out by Matlab to perform the feature reduction part and the resulted feature vector is then transmitted to the Zynq FPGA to perform training and implementation of the multi-layer perceptron that performs the classification part.

3- Conclusions

The recent directions dealt with a ECG-FPGA systems is introduced in this paper. These directions involve the utilization of the FPGA-based hardware solutions to address several problems in medicine and health care field, especially those related to the ECG signal field aspects, which in turn give a great design and implementation flexibility. The benefits of this were clearly visible in purposing different FPGA-based hardware solutions that might be able to replace costly and bigger medical equipment with relatively cheap, much lighter and possibly portable systems that based on FPGA while maintain or even enhance high performance and response speed.

On the other hand, the implementation of ECG-FPGA systems makes it possible to deal with variety of ECG aspects. For instant, recent approaches focus on aspects related to security issues of ECG access and transmission, efficient ECG data compression, noise and interference effect removal, as well as improving detection and diagnose.

In addition, it's clear that FPGA high design flexibility and fast performance will provide the ability to address a new research aspect and present efficient solutions for a future ECG systems enchantments and challenges.

CONFLICT OF INTERESTS.

- There are no conflicts of interest.

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بحث استقصائي: الاتجاهات الحديثة في بحوث ال ECG-FPGA

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الخلاصة

لقد شهدت السنوات القليلة الماضية اهتماماً متزايداً نحو استخدام مصفوفة البوابات المنطقية القابلة للبرمجة FPGA في التطبيقات المختلفة. لقد أدى التقدم الحاصل في مرونة التعامل مع الموارد بالاضافة الى الزيادة في سرعة الاداء وانخفاض الثمن للـــ FPGA وكذلك الاستهلاك القليل للطاقة الى هذا الاهتمام المتزايد بالـــ FPGA. ان استخدام الـــ FPGA في مجالات الطب والصحة يهدف بشكل عام الى استبدال اجهزة المراقبة الطبية كبيرة الحجم وغالية الثمن باخرى أصغر حجماً مع امكانية تصميمها لكي تكون اجهزة محمولة اعتماداً على مرونة التصميم التي يوفرها الـــ FPGA. إنصب الاهتمام في العديد من البحوث الحالية على استخدام نظام FPGA لمعالجة الجوانب المتعلقة بإشارة تخطيط القلب وذلك لتوفير التحسينات في الاداء وزيادة السرعة بالاضافة الى أيجاد وإقتراح افكار جديدة لمثل هذه التطبيقات. ان هذا البحث يوفر نظرة عامة عن الاتجاهات الحالية في انظمة ECG-FPGA.

الكلمات الداله:- الأمن، ضغط، تقليل الضوضاء، الكشف، التشخيص.